

## PATENT ABSTRACTS OF JAPAN

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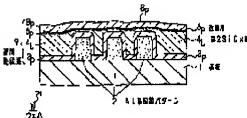
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## (54) FORMATION OF SILICON OXIDE DIELECTRIC FILM

## (57)Abstract:

**PROBLEM TO BE SOLVED:** To provide a silicon oxide dielectric film which can be used as an interlayer insulating film in a semiconductor device and can realize both a low dielectric constant and a long-term reliability.

**SOLUTION:** With use of a monomethyl silane/hydrogen peroxide film-forming gas, a first moisture-resistive SiOx film 3P is formed directly on an Al-based wiring pattern 2 by a plasma CVD process, and a second SiOx film 4L having a high fluidity for reducing a step difference on a surface of a wafer W is formed on the film 3P by a low-temperature, low-pressure (LPCVD) process. A modified layer 6P may be formed by an oxygen plasma modification process on the second SiOx film 4L, and further a third SiOx film 8P may be formed on the modified layer 6P by the plasma CVD process with use of the same film-forming gas as the above. Any of the SiOx films 3P, 4L and 8P is lower in relative permittivity than a silicon oxide film of a stoichiometric composition obtained by thermally oxidizing silicon, and thus the overall relative permittivity of an interlayer insulating film 9 can be kept low.



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CLAIMS

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[Claim(s)]

[Claim 1]A formation method of a silicon oxide system dielectric film characterized by comprising the following.  
The 1st process of forming the 1st dielectric film whose specific inductive capacity is lower than a silicon oxide film of a stoichiometric composition acquired by oxidizing silicon thermally by plasma CVD so that a metal wiring pattern on a base may be covered.

The 2nd process of forming the 2nd dielectric film whose specific inductive capacity is still lower than said 1st dielectric film by performing decompression CVD using forming gas used by said plasma CVD, and forming gas which consists of the same ingredient so that a surface step of a base may be eased on this 1st dielectric film.

[Claim 2]A formation method of the silicon oxide system dielectric film according to claim 1 using what does not contain gas constituents which use fluoride as a composing element as said forming gas.

[Claim 3]A formation method of the silicon oxide system dielectric film according to claim 1 performing plasma modification processing for stiffening the surface after forming said 2nd dielectric film.

[Claim 4]By performing plasma CVD again using forming gas used by said plasma CVD after forming said 2nd dielectric film, and forming gas which consists of the same ingredient, A formation method of the silicon oxide system dielectric film according to claim 1 forming the 3rd dielectric film whose specific inductive capacity is lower than a thermal oxidation silicone film produced by oxidizing silicon thermally on this 2nd dielectric film.

[Claim 5]By performing plasma modification processing for stiffening the surface after forming said 2nd dielectric film, and performing plasma CVD again using forming gas used for after an appropriate time by said plasma CVD, and forming gas which consists of the same ingredient, A formation method of the silicon oxide system dielectric film according to claim 1 forming the 3rd dielectric film whose specific inductive capacity is lower than a silicon oxide film of a stoichiometric composition acquired by oxidizing silicon thermally on this 2nd dielectric film.

[Claim 6]A formation method of the silicon oxide system dielectric film according to claim 1 using gas by which at least one of a hydrogen atom of the Silang system compound contains an organic silane compound replaced by a hydrocarbon group, and an oxidizer as forming gas of plasma CVD for forming said 1st dielectric film.

[Claim 7]A formation method of the silicon oxide system dielectric film according to claim 6 using a monomethyl silane as said organic silane compound, and using hydrogen peroxide as said oxidizer.

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## DETAILED DESCRIPTION

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[Detailed Description of the Invention]

[0001]

[Field of the Invention]This invention relates to the method of reconciling membranous lower-dielectric-constant-izing and long term reliability especially, about the formation method of the dielectric film used as an interlayer insulation film of a semiconductor device.

[0002]

[Description of the Prior Art]In semiconductor device manufacture in recent years, adoption of the multilevel interconnection art which accumulates a metal wiring pattern via an interlayer insulation film with the high integration and advanced features at many layers on a substrate is indispensable. If adjacent wires or up-and-down wiring approach with reduction of a design rule when adopting multilevel interconnection, in the specific inductive capacity epsilon, in about 3.9 and the conventional large SiO<sub>2</sub> system interlayer insulation film, the capacity between wiring will become large too much. then -- especially -- design rule 0.25micrometer -- realizing a low voltage drive, low power consumption, and a high clock frequency using a dielectric film with low specific inductive capacity (a low dielectric film is called hereafter.) is examined by subsequent generations.

[0003]As a low dielectric film, the organic system low dielectric film and the inorganic system low dielectric film are examined until now. First of all, since the electronegativity of O atom under siloxane (-Si-O-) combination in which, as for about 3.9 and a large thing, the specific inductive capacity epsilon of SiO<sub>2</sub> makes the skeleton of SiO<sub>2</sub> is large, the electron inclines toward the O atom side.

It is because the bias will increase further if an electric field is given.

Therefore, decline in polarizability is indispensable to lower-dielectric-constant-izing. In that respect, by the organic system low dielectric film, since the large alkyl group of steric exclusion exists, the density of a film and the polarizability of the molecule itself are falling, and thereby, decline in specific inductive capacity is brought about. For example, specific inductive capacity epsilon= 3.5-3.0 is attained by the polyimide system resin layer, and the value of epsilon= 2.7-1.9 is attained by the fluororesin film.

[0004]On the other hand, as an inorganic system low dielectric film, the SiOF film which can form membranes by plasma CVD, i.e., the SiOx film containing F (fluoride), is mainly examined. The specific inductive capacity of a SiOF film decreases with the increase in F concentration in a film, and about 3.7 to 3.2 value is attained until now. The reason for falling, when the specific inductive capacity of SiOx contains F is considered for the both sides of the electronic polarization resulting from distortion of an electron cloud and the ionic polarization resulting from nuclear displacement to decrease in number although not fully solved yet.

[0005]

[Problem(s) to be Solved by the Invention]However, the above-mentioned organic system low dielectric film and

the inorganic system dielectric film are holding the problem in each. First, in an organic system low dielectric film, after carrying out the spin coat of the polymeric material dissolved in the solvent on a base, are formed by many by heating this coat and carrying out a drying polymerization. In such a film, water and the solvent which were generated at the time of a polymerization are easy to be incorporated into a film, and these water and solvents become the cause of making a metal wiring pattern corroding. If polymer polymerization is made to attain by a radical polymerization, since the problem of water or a solvent is not produced, films, such as a fluorinated-amorphous-carbon film which can form membranes by plasma CVD, are also proposed. However, since the foundations of a molecular skeleton are chains, an organic layer is intrinsically inferior in oxygen plasma tolerance, and causing film decrease at the time of resist-ashing after a contact hole opening poses a problem. [0006] On the other hand, it absorbs moisture quickly during air neglect, and the problem of degrading the stability of the film itself or a process is among the SiOF films which are the examples of representation of an inorganic system low dielectric film. Not only making a metal wiring pattern corrode but the fluoric acid (HF) produced according to moisture absorption this, it is because pH of polishing slurry in case a semiconductor manufacturing device is made to pollute and corrode or CMP (chemical machinery polish) performs flattening of an interlayer insulation film is changed and polishing speed is fluctuated as a result. Si(-F)<sub>2</sub> combination considered that two F atoms combined with one Si atom by the hygroscopic high film, Si-F combination considered to have approached via O atom exists, these combination changes to Si-OH combination through a hydrolysis reaction, and when this Si-OH combination forms a hydrogen bond between H<sub>2</sub>O in the atmosphere, it is thought that moisture absorption advances.

[0007] Therefore, under the present circumstances, it is very difficult to also use an organic system low dielectric film and inorganic matter system low dielectric film as an interlayer insulation film alone. For this reason, the interlayer insulation film of the bipolar membrane composition which sandwiched the upper and lower sides of the low dielectric film which are excellent in mobility with the SiO<sub>2</sub> film which is comparatively excellent in membrane quality although specific inductive capacity is slightly high, or the SiN film is proposed. For example, in 1995 to the dry process symposium abstract collection p.261-268. The interlayer insulation film which covers an Al wiring pattern is made into order with 3 lamination of a base layer, a flow layer, and a cap layer from the lower layer side. A base layer and a cap layer are plasma CVD with a substrate temperature of 300 °C using a SiH<sub>4</sub>/N<sub>2</sub>O/N<sub>2</sub> mixed gas system. The method of a flow layer forming by the decompression CVD (LPCVD) with a substrate temperature of 0 °C using a SiH<sub>4</sub>/H<sub>2</sub>O<sub>2</sub>/N<sub>2</sub> system, respectively is proposed. In the monthly semiconductor world February, 1996 item p.86-88 (press journal company \*\*). The interlayer insulation film which covers an Al wiring pattern is made into 3 lamination of a barrier film, a SiOF film, and a barrier film from a lower layer at order, and the method of using a SiO<sub>2</sub> film as this barrier film is indicated. In addition, to insert the upper and lower sides of the organic system low dielectric film of a coating mold with the SiO<sub>2</sub> film which is comparatively excellent in membrane quality, or an SiN film is also tried widely.

[0008] However, each material which constitutes the above-mentioned base layer, a cap layer, and a barrier layer from such bipolar membrane formation art is a SiO<sub>2</sub> film with high specific inductive capacity, or an SiN film whose specific inductive capacity is still higher than this, and the limit has produced in decline in the specific inductive capacity as the whole interlayer insulation film. When the upper and lower sides of the fluid high film which contains moisture in a film are inserted by a film with little moisture, in order to protect the metal wiring pattern of the bottom about the film by the side of the function to make moisture penetrate to the upper part about the film by the side of the upper layer, and a lower layer, the characteristic of not making moisture penetrating to the bottom was required, and there was a problem that selection of the optimal membrane type was difficult.

Then, this invention solves this hygroscopic problem and an object of this invention is to provide the method of forming the dielectric film which lower dielectric constant-ization is attained and is excellent also in long term reliability.

[0009]

[Means for Solving the Problem]In a formation method of a silicon oxide system dielectric film of this invention. A good film of membraneous quality is allotted to a portion which touches a metal wiring pattern on a base directly. Although the conventional view of specific inductive capacity covering moreover with a low fluid high film, and planning flatness of a base is followed, Adopt what has specific inductive capacity lower than a silicon oxide film of a stoichiometric composition acquired by each oxidizing silicon thermally as each film, and a dielectric constant of the whole interlayer insulation film is maintained low, And the above-mentioned purpose is attained by taking a simple technique of forming and dividing each film by a different CVD condition using forming gas which consists of the same ingredient, i.e., plasma CVD, and LPCVD. That is, after forming the 1st dielectric film that covers a metal wiring pattern by plasma CVD, the 2nd dielectric film that eases a surface step of a base on it is formed by LPCVD.

[0010]In this invention, forming gas containing gas constituents which use fluoride as a composing element is not used. That is, a silicon oxide system dielectric film formed of this invention does not expect lower dielectric constant-ization by incorporating a fluorine atom into a film like a SiOF film. After forming the 2nd dielectric film, the 3rd dielectric film may be further laminated by performing plasma CVD again using forming gas which could perform plasma modification processing for stiffening the surface, or was used by previous plasma CVD, and forming gas which consists of the same ingredient. Specific inductive capacity of this 3rd dielectric film is also lower than a silicon oxide film of a stoichiometric composition naturally acquired by oxidizing silicon thermally. Or both laminations of plasma modification processing of the surface of the 2nd dielectric film and the 3rd dielectric film to an it top may be performed.

[0011]

[Embodiment of the Invention]Even if the forming gas which consists of the same ingredient is used for this invention, paying attention to the membraneous quality of a dielectric film changing with CVD conditions, it is simple and tends to realize formation of a controllable high dielectric film. In plasma CVD, since [ which an ion weld slag operation commits to a film ] it is and the density of a film rises, large lower dielectric constant-ization cannot be expected. However, on the other hand, there are very few moisture contents that film formation is intrinsically due to the radical polymerization reaction, and by the drying effect by ion weld slag operation being expectable, and the dielectric film which has precise membraneous quality can be formed. This film is convenient as the 1st dielectric film that covers a metal wiring pattern first and protects this, or the 3rd dielectric film that covers the uppermost surface of an interlayer insulation film and plays the role of passivation. The specific inductive capacity of this 1st dielectric film and the 3rd dielectric film, Since it is lower than the specific inductive capacity (about 3.9) of the silicon oxide film of the stoichiometric composition acquired by oxidizing silicon thermally, it is possible to lower the specific inductive capacity as the whole interlayer insulation film compared with the case where the upper and lower sides of a low dielectric film are inserted by a  $\text{SiO}_2$  film like before.

[0012]Since the migration of the membrane formation kind in the part and membrane surface which a physical action like an ion weld slag operation does not commit on a film by an LPCVD method on the other hand is promoted, A dielectric film with a sufficient coverage can be formed, and since the density of a film moreover does not become so high, specific inductive capacity can be lowered. This film is convenient as the 2nd dielectric film contributed to the substantial decline in the specific inductive capacity of the whole interlayer insulation film, easing the surface step of the base resulting from a metal wiring pattern.

[0013]Since above plasma CVD and LPCVD(s) are performed in this invention using the forming gas which

consists of the same ingredient, Chemical composition is fundamentally common although there is a difference of some of the elemental ratio according [ the 1st dielectric film and the 2nd dielectric film which are formed, or the 3rd dielectric film added if needed ] to a film formation condition. Therefore, unlike the case where a completely different film of chemical composition of a different kind is laminated, it becomes, without causing difficulty to selection of a membrane type.

[0014] If the forming gas which does not contain the gas constituents which use fluoride (F) as a composing element is used when forming the 3rd dielectric film the 1st dielectric film, the 2nd dielectric film, or if needed in this invention, F can be eliminated from a film. Therefore, all the problems of the variation in the polishing speed in generation of fluoric acid (HF) by membranous moisture absorption, the corrosion of the metal wiring pattern by this, and CMP are avoidable. It is preferred for above plasma CVD and LPCVD to carry out continuously, without carrying out atmosphere release of the base over a long time on the way. However, the forming temperature of these CVD(s) [ both ] differs greatly, and if it tries to perform both CVD(s) by the same chamber succeeding the case where the temperature control of the stage which lays this base is moreover performing heating of a base, the loss of the time accompanying the temperature control of a stage will become large. Therefore, in such a case, it is preferred to use the multi chamber type device with which the plasma CVD chamber which differs in stage temperature setting out beforehand, and the LPCVD chamber were made to connect by a vacuum carrying path.

[0015] It is preferred that at least one of the hydrogen atom of the Silang system compound uses the gas containing the organic silane compound replaced by the hydrocarbon group and an oxidizer as forming gas for plasma CVD for forming the 1st dielectric film or the 3rd dielectric film added if needed. The basic skeleton of the above-mentioned organic silane compound may be mono-silane  $\text{SiH}_4$ , or may be polysilane, such as disilane  $\text{Si}_2\text{H}_6$ . The carbon number in particular of the hydrocarbon group which replaces the hydrogen atom of these Silang system compound is not limited. Although based also on the number of substitution, it is expectable that film density falls [ the one where a carbon number is to some extent larger ] according to increase of the steric exclusion of a hydrocarbon group as a general tendency, and specific inductive capacity falls, and the mobility of the membrane formation intermediate in a film growth process improves. The carbon content of the dielectric film which will be obtained on the other hand if a carbon number is not much large increases, moisture resistance deteriorates, satisfying membranous quality becomes not easily obtained by plasma CVD, either, and also it becomes difficult to deal with an organic silane compound as a gas. Therefore, as a hydrocarbon group which replaces the hydrogen atom of the Silang system compound, allyl groups, such as alkyl groups of 1-2 carbon numbers, such as a methyl group and an ethyl group, or a phenyl group, are suitable. On the other hand, as the above-mentioned oxidizer, oxygen ( $\text{O}_2$ ), ozone ( $\text{O}_3$ ), hydrogen peroxide ( $\text{H}_2\text{O}_2$ ), etc. can be used.

[0016] In particular, it is organicity. It is a monomethyl silane as a silane compound.  $[\text{Si}(\text{CH}_3) \text{H}_3]$  When  $\text{H}_2\text{O}_2$  is used as an oxidizer, the dielectric film of the form where carbon was incorporated into the  $\text{SiO}_2$  film of the stoichiometric composition acquired by the thermal oxidation of silicon can be obtained. The applicant for this patent has found out that the mobility of a membrane formation intermediate improves about this  $\text{Si}(\text{CH}_3) \text{H}_3/\text{H}_2\text{O}_2$  system when forming temperature is 20 ° or less in LPCVD before. It has been thought that it is inferior to membranous quality while the dielectric film containing the carbon formed by the above systems of reaction is more advantageous to lower-dielectric-constant-izing than before. However, if membrane formation which switched plasma CVD and LPCVD like this invention is performed, even if it is such the system of reaction, good membranous quality and lower dielectric constant can be reconciled.

[0017]

[Example] Hereafter, the concrete example of this invention is described.

[0018] Example 1 -- here, this invention being applied to formation of the interlayer insulation film in a semiconductor wafer process, and, By performing the plasma CVD and LPCVD by an  $\text{Si}(\text{CH}_3)_2\text{H}_2/\text{H}_2\text{O}_2$  system continuously, the  $\text{SiO}_x$  system interlayer insulation film of two-layer composition with low specific inductive capacity was formed. This example of a process is explained referring to drawing 1 and drawing 2. The device used by this example is connected common to one set of the object for plasma CVD, the object for LPCVD, and the wafer handling unit by which each of the chamber for post annealing was maintained by the predetermined degree of vacuum. It is the multi chamber-type device made as [perform / conveyance of the base between each chamber / altogether / via this wafer handling unit].

[0019] The wafer W in which 0.65-micrometer-high aluminum system circuit pattern 2 was first formed [on the substrate 1] according to the line and space which is 0.4 micrometer as a metal wiring pattern beforehand was prepared. Among the above-mentioned substrate 1, although a field corresponding directly under aluminum system circuit pattern 2 comprises an insulator layer, the structure under the common metallic wiring of the usual semiconductor device is not illustrated here.

[0020] Next, this wafer W was carried in to the plasma CVD device, and plasma CVD was performed on condition of the following as an example.

$\text{Si}(\text{CH}_3)_2\text{H}_2$  flow 100 SCCM Ar flow 500 SCCM  $\text{H}_2\text{O}_2$  (gas) speed of supply A part for 0.7 g / Pressure 160 Pa RF power 200 W (13.56 MHz)

1st  $\text{SiO}_x$  film 3<sub>p</sub> with a thickness of about 0.1 micrometer which covers aluminum system circuit pattern 2 to conformal one mostly as it can wafer-temperature 350 °C. Come, and is alike and it is shown more in drawing 1 (it means that the subscript P relates to a plasma process.) It is the same as that of the following. Membranes were formed. The specific inductive capacity of this 1st  $\text{SiO}_x$  film 3<sub>p</sub> was a little lower than the specific inductive capacity  $\epsilon_{\text{SiO}_2}$  of the  $\text{SiO}_2$  film of the stoichiometric composition acquired by the thermal oxidation of silicon. This is an effect of the methyl group incorporated into the film.

[0021] Next, the above-mentioned wafer W was conveyed to the LPCVD device under the high vacuum, and LPCVD was performed on condition of the following as an example.

$\text{Si}(\text{CH}_3)_2\text{H}_2$  flow 100 SCCM Ar flow 500 SCCM  $\text{H}_2\text{O}_2$  (gas) speed of supply 0.7 g / part pressure 133 Pa wafer temperature 0 °C -- thereby, it is 2nd  $\text{SiO}_x$  film 4<sub>L</sub> (it means that the subscript L relates to a LPCVD process.)

about 0.1 micrometer thick so that the surface step of the base resulting from aluminum system circuit pattern 2 may be canceled mostly, as shown in drawing 2. It is the same as that of the following. Membranes were formed. The specific inductive capacity of this 2nd  $\text{SiO}_x$  film 4<sub>L</sub> was still lower than the dielectric constant of the above-mentioned 1st  $\text{SiO}_x$  film 3<sub>p</sub>.

[0022] Then, the chamber for post annealing was conveyed for the wafer W, 400 °C and post annealing for 15 minutes were performed among  $\text{N}_2$  atmosphere of  $1.01 \times 10^5$  Pa, and the moisture which remains in the film of 2nd  $\text{SiO}_x$  film 4<sub>L</sub> was removed. The specific inductive capacity  $\epsilon$  of the interlayer insulation film 5 measured in this stage, i.e., the film which doubled the above-mentioned 1st  $\text{SiO}_x$  film 3<sub>p</sub> and 2nd  $\text{SiO}_x$  film 4<sub>L</sub>, was about 3.2. Although the acceleration deterioration test of 1000 hours under the relative humidity of 100%, the temperature of 120 °C, and humid high-temperature-high-pressure environment with a pressure of 2 atmospheres was done to the base of this state, neither the corrosion of aluminum system circuit pattern 2 nor degradation of hot carrier tolerance was accepted at all. Therefore, it was proved that the above-mentioned interlayer insulation film 5 had specific inductive capacity low as a whole, and was excellent also in moisture resistance.

[0023]In example 2 this example, surface treatment processing by oxygen plasma was performed to 2nd SiOx film 4<sub>L</sub> formed in Example 1. Here the used device between each chamber the object for plasma CVD, the object for LPCVD, for plasma treatment, and for post annealing, It is the multi chamber-type device made as [ perform / conveyance of the base between each chamber / it is connected to the wafer handling unit by which the base was maintained at the high vacuum, and / altogether / via this wafer handling unit ].

[0024]The stage film formation of the above-mentioned 2nd SiOx film 4<sub>L</sub> is as having mentioned above in Example 1. In this example, the following conditions performed oxygen plasma treatment as opposed to this film continuously.

O<sub>2</sub> flow 2000 SCCM Ar flow 1000 SCCM Pressure 133 Pa RF power 500 W (13.56 MHz)

wafer temperature 350 °C processing time a part for three – of this plasma treatment, by the layer part of 2nd SiOx film 4<sub>L</sub>, eburnation of drying and a film advanced and reforming layer 6<sub>p</sub> as shown in drawing 3 was formed.

Since the wafer temperature at the time of the above-mentioned plasma treatment is the same as the wafer temperature at the time of membrane formation of 1st SiOx film 3<sub>p</sub> by the above-mentioned plasma CVD, It can be considered as the chamber for plasma CVD, and common use, without providing the above-mentioned chamber for plasma treatment separately, and can also respond by the change of the gas supplied to a chamber, RF power, and an exhaust speed.

[0025]Then, the same post annealing as Example 1 was performed to the above-mentioned wafer W. In this example, the interlayer insulation film 7 which consists of three persons of 1st SiOx film 3<sub>p</sub>, 2nd SiOx film 4<sub>L</sub>, and reforming layer 6<sub>p</sub> was formed. The specific inductive capacity epsilon as this whole interlayer insulation film 7 was about 3.3. Since the rise of the specific inductive capacity by the densification of reforming layer 6<sub>p</sub> influenced, it is thought of that the specific inductive capacity epsilon became a little higher than Example 1. The result of the acceleration deterioration test of this interlayer insulation film 7 was better than Example 1.

[0026]In example 3 this example, after performing even formation of reforming layer 6<sub>p</sub> like above-mentioned Example 2, the 3rd dielectric film by plasma CVD was further laminated on this. That is, the wafer W of the state which showed in drawing 3 shown above was again returned to the plasma CVD device used for membrane formation of 1st SiOx film 3<sub>p</sub>, and plasma CVD was performed on condition of the following as an example.

Si(CH<sub>3</sub>)<sub>2</sub> H<sub>2</sub> flow 80 SCCM Ar flow 500 SCCM H<sub>2</sub>O<sub>2</sub> (gas) speed of supply a part for 0.85g/– pressure 93 Pa wafer temperature 350 °C – thereby, 3rd SiOx film 8<sub>p</sub> as shown in drawing 4 was formed at the thickness which is about 0.3 micrometer.

[0027]Then, the same post annealing as Example 1 was performed to the above-mentioned wafer W. In this example, the interlayer insulation film 9 which consists of four persons of 1st SiOx film 3<sub>p</sub>, 2nd SiOx film 4<sub>L</sub>, reforming layer 6<sub>p</sub>, and 3rd SiOx film 8<sub>p</sub> was formed. The specific inductive capacity epsilon as this whole interlayer insulation film 9 was about 3.6. It is because 3rd SiOx film 8<sub>p</sub> with membraneous quality there are few carbon contents and precise [ that this specific inductive capacity epsilon rose further rather than Example 2 ] and high specific inductive capacity was added. The result of the acceleration deterioration test of this interlayer insulation film 9 was still better than Example 2.

[0028]As mentioned above, although this invention was explained based on the example of three examples, this invention is not limited to these examples at all, and change, selection, and combination are possible for it suitably about details, such as composition of a sample wafer, a size of each part, a film formation condition, plasma treatment conditions, and a post annealing condition.



[0029]

[Effect of the Invention] Even when it is advantageous to lower-dielectric-constant-izing, according to this invention, it becomes possible [ also applying the difficult conventional system of reaction to the membrane formation of a dielectric film which has the membraneous quality outstanding according to the film formation condition ] to desire high membraneous quality-ization, so that clearly also from the above explanation. Therefore, a dielectric film can consist of  $\text{SiO}_2$  films of the stoichiometric composition acquired by the thermal oxidation of silicon only using a film with small specific inductive capacity, without putting the upper and lower sides of a low dielectric film by a film with high specific inductive capacity like a  $\text{SiO}_2$  film or an  $\text{SiN}$  film. When this invention is applied to membrane formation of the interlayer insulation film in the manufacturing process of a semiconductor device, lower-dielectric-constant-izing of this interlayer insulation film and improvement in long term reliability are compatible, and an obstacle when this realizes high integration and improvement in the speed of operation of a semiconductor device is conquered.

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TECHNICAL FIELD

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[Field of the Invention]This invention relates to the method of reconciling membranous lower-dielectric-constant-izing and long term reliability especially, about the formation method of the dielectric film used as an interlayer insulation film of a semiconductor device.

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PRIOR ART

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[Description of the Prior Art]In semiconductor device manufacture in recent years, adoption of the multilevel interconnection art which accumulates a metal wiring pattern via an interlayer insulation film with the high integration and advanced features at many layers on a substrate is indispensable. If adjacent wires or up-and-down wiring approach with reduction of a design rule when adopting multilevel interconnection, in the specific inductive capacity epsilon, in about 3.9 and the conventional large SiO<sub>2</sub> system interlayer insulation film, the capacity between wiring will become large too much. then -- especially -- design rule 0.25micrometer -- realizing a low voltage drive, low power consumption, and a high clock frequency using a dielectric film with low specific inductive capacity (a low dielectric film is called hereafter.) is examined by subsequent generations. [0003]As a low dielectric film, the organic system low dielectric film and the inorganic system low dielectric film are examined until now. First of all, since the electronegativity of O atom under siloxane (-Si-O-) combination in which, as for about 3.9 and a large thing, the specific inductive capacity epsilon of SiO<sub>2</sub> makes the skeleton of SiO<sub>2</sub> is large, the electron inclines toward the O atom side.

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EFFECT OF THE INVENTION

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[Effect of the Invention]Even when it is advantageous to lower-dielectric-constant-izing, according to this invention, it becomes possible [ also applying the difficult conventional system of reaction to the membrane formation of a dielectric film which has the membraneous quality outstanding according to the film formation condition ] to desire high membraneous quality-ization, so that clearly also from the above explanation. Therefore, a dielectric film can consist of  $\text{SiO}_2$  films of the stoichiometric composition acquired by the thermal oxidation of silicon only using a film with small specific inductive capacity, without putting the upper and lower sides of a low dielectric film by a film with high specific inductive capacity like a  $\text{SiO}_2$  film or an  $\text{SiN}$  film. When this invention is applied to membrane formation of the interlayer insulation film in the manufacturing process of a semiconductor device, lower-dielectric-constant-izing of this interlayer insulation film and improvement in long term reliability are compatible, and an obstacle when this realizes high integration and improvement in the speed of operation of a semiconductor device is conquered.

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**TECHNICAL PROBLEM**


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[Problem(s) to be Solved by the Invention]However, the above-mentioned organic system low dielectric film and the inorganic system dielectric film are holding the problem in each. First, in an organic system low dielectric film, after carrying out the spin coat of the polymeric material dissolved in the solvent on a base, are formed by many by heating this coat and carrying out a drying polymerization. In such a film, water and the solvent which were generated at the time of a polymerization are easy to be incorporated into a film, and these water and solvents become the cause of making a metal wiring pattern corroding. If polymer polymerization is made to attain by a radical polymerization, since the problem of water or a solvent is not produced, films, such as a fluorinated-amorphous-carbon film which can form membranes by plasma CVD, are also proposed. However, since the foundations of a molecular skeleton are chains, an organic layer is intrinsically inferior in oxygen plasma tolerance, and causing film decrease at the time of resist-ashing after a contact hole opening poses a problem. [0006]On the other hand, it absorbs moisture quickly during air neglect, and the problem of degrading the stability of the film itself or a process is among the SiOF films which are the examples of representation of an inorganic system low dielectric film. Not only making a metal wiring pattern corrode but the fluoric acid (HF) produced according to moisture absorption this, it is because pH of polishing slurry in case a semiconductor manufacturing device is made to pollute and corrode or CMP (chemical machinery polish) performs flattening of an interlayer insulation film is changed and polishing speed is fluctuated as a result. Si(-F)<sub>2</sub> combination considered that two F atoms combined with one Si atom by the hygroscopic high film, Si-F combination considered to have approached via O atom exists, these combination changes to Si-OH combination through a hydrolysis reaction, and when this Si-OH combination forms a hydrogen bond between H<sub>2</sub>O in the atmosphere, it is thought that moisture absorption advances.

[0007]Therefore, under the present circumstances, it is very difficult to also use an organic system low dielectric film and inorganic matter system low dielectric film as an interlayer insulation film alone. For this reason, the interlayer insulation film of the bipolar membrane composition which sandwiched the upper and lower sides of the low dielectric film which are excellent in mobility with the SiO<sub>2</sub> film which is comparatively excellent in membrane quality although specific inductive capacity is slightly high, or the SiN film is proposed. For example, in 1995 to the dry process symposium abstract collection p.261-268. The interlayer insulation film which covers an Al wiring pattern is made into order with 3 lamination of a base layer, a flow layer, and a cap layer from the lower layer side, A base layer and a cap layer are plasma CVD with a substrate temperature of 300 °C using a SiH<sub>4</sub>/N<sub>2</sub>O/N<sub>2</sub> mixed gas system, The method of a flow layer forming by the decompression CVD (LPCVD) with a substrate temperature of 0 °C using a SiH<sub>4</sub>/H<sub>2</sub>O<sub>2</sub>/N<sub>2</sub> system, respectively is proposed. In the monthly semiconductor world February, 1996 item p.86-88 (press journal company °C). The interlayer insulation film which covers an Al wiring pattern is made into 3 lamination of a barrier film, a SiOF film, and a barrier film from a lower

layer at order, and the method of using a  $\text{SiO}_2$  film as this barrier film is indicated. In addition, to insert the upper and lower sides of the organic system low dielectric film of a coating mold with the  $\text{SiO}_2$  film which is comparatively excellent in membraneous quality, or an  $\text{SiN}$  film is also tried widely.

[0008] However, each material which constitutes the above-mentioned base layer, a cap layer, and a barrier layer from such bipolar membrane formation art is a  $\text{SiO}_2$  film with high specific inductive capacity, or an  $\text{SiN}$  film whose specific inductive capacity is still higher than this, and the limit has produced in decline in the specific inductive capacity as the whole interlayer insulation film. When the upper and lower sides of the fluid high film which contains moisture in a film are inserted by a film with little moisture, In order to protect the metal wiring pattern of the bottom about the film by the side of the function to make moisture penetrate to the upper part about the film by the side of the upper layer, and a lower layer, the characteristic of not making moisture penetrating to the bottom was required, and there was a problem that selection of the optimal membrane type was difficult. Then, this invention solves this hygroscopic problem and an object of this invention is to provide the method of forming the dielectric film which lower dielectric constant-ization is attained and is excellent also in long term reliability.

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MEANS

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[Means for Solving the Problem]In a formation method of a silicon oxide system dielectric film of this invention. A good film of membraneous quality is allotted to a portion which touches a metal wiring pattern on a base directly, Although the conventional view of specific inductive capacity covering moreover with a low fluid high film, and planning flatness of a base is followed, Adopt what has specific inductive capacity lower than a silicon oxide film of a stoichiometric composition acquired by each oxidizing silicon thermally as each film, and a dielectric constant of the whole interlayer insulation film is maintained low, And the above-mentioned purpose is attained by taking a simple technique of forming and dividing each film by a different CVD condition using forming gas which consists of the same ingredient, i.e., plasma CVD, and LPCVD. That is, after forming the 1st dielectric film that covers a metal wiring pattern by plasma CVD, the 2nd dielectric film that eases a surface step of a base on it is formed by LPCVD.

[0010]In this invention, forming gas containing gas constituents which use fluoride as a composing element is not used. That is, a silicon oxide system dielectric film formed of this invention does not expect lower dielectric constant-ization by incorporating a fluorine atom into a film like a SiOF film. After forming the 2nd dielectric film, the 3rd dielectric film may be further laminated by performing plasma CVD again using forming gas which could perform plasma modification processing for stiffening the surface, or was used by previous plasma CVD, and forming gas which consists of the same ingredient. Specific inductive capacity of this 3rd dielectric film is also lower than a silicon oxide film of a stoichiometric composition naturally acquired by oxidizing silicon thermally. Or both laminations of plasma modification processing of the surface of the 2nd dielectric film and the 3rd dielectric film to an it top may be performed.

[0011]

[Embodiment of the Invention]Even if the forming gas which consists of the same ingredient is used for this invention, paying attention to the membraneous quality of a dielectric film changing with CVD conditions, it is simple and tends to realize formation of a controllable high dielectric film. In plasma CVD, since [ which an ion weld slag operation commits to a film ] it is and the density of a film rises, large lower dielectric constant-ization cannot be expected. However, on the other hand, there are very few moisture contents that film formation is intrinsically due to the radical polymerization reaction, and by the drying effect by ion weld slag operation being expectable, and the dielectric film which has precise membraneous quality can be formed. This film is convenient as the 1st dielectric film that covers a metal wiring pattern first and protects this, or the 3rd dielectric film that covers the uppermost surface of an interlayer insulation film and plays the role of passivation. The specific inductive capacity of this 1st dielectric film and the 3rd dielectric film, Since it is lower than the specific inductive capacity (about 3.9) of the silicon oxide film of the stoichiometric composition acquired by oxidizing silicon thermally, it is possible to lower the specific inductive capacity as the whole interlayer insulation film compared with the case where the upper and lower sides of a low dielectric film are inserted by a  $\text{SiO}_2$  film like before.

[0012] Since the migration of the membrane formation kind in the part and membrane surface which a physical action like an ion weld slag operation does not commit on a film by an LPCVD method on the other hand is promoted, A dielectric film with a sufficient coverage can be formed, and since the density of a film moreover does not become so high, specific inductive capacity can be lowered. This film is convenient as the 2nd dielectric film contributed to the substantial decline in the specific inductive capacity of the whole interlayer insulation film, easing the surface step of the base resulting from a metal wiring pattern.

[0013] Since above plasma CVD and LPCVD(s) are performed in this invention using the forming gas which consists of the same ingredient, Chemical composition is fundamentally common although there is a difference of some of the elemental ratio according [ the 1st dielectric film and the 2nd dielectric film which are formed, or the 3rd dielectric film added if needed ] to a film formation condition. Therefore, unlike the case where a completely different film of chemical composition of a different kind is laminated, it becomes, without causing difficulty to selection of a membrane type.

[0014] If the forming gas which does not contain the gas constituents which use fluoride (F) as a composing element is used when forming the 3rd dielectric film the 1st dielectric film, the 2nd dielectric film, or if needed in this invention, F can be eliminated from a film. Therefore, all the problems of the variation in the polishing speed in generation of fluoric acid (HF) by membranous moisture absorption, the corrosion of the metal wiring pattern by this, and CMP are avoidable. It is preferred for above plasma CVD and LPCVD to carry out continuously, without carrying out atmosphere release of the base over a long time on the way. However, the forming temperature of these CVD(s) [ both ] differs greatly, and if it tries to perform both CVD(s) by the same chamber succeeding the case where the temperature control of the stage which lays this base is moreover performing heating of a base, the loss of the time accompanying the temperature control of a stage will become large. Therefore, in such a case, it is preferred to use the multi chamber type device with which the plasma CVD chamber which differs in stage temperature setting out beforehand, and the LPCVD chamber were made to connect by a vacuum carrying path.

[0015] It is preferred that at least one of the hydrogen atom of the Silang system compound uses the gas containing the organic silane compound replaced by the hydrocarbon group and an oxidizer as forming gas for plasma CVD for forming the 1st dielectric film or the 3rd dielectric film added if needed. The basic skeleton of the above-mentioned organic silane compound may be mono-silane  $\text{SiH}_4$ , or may be polysilane, such as disilane  $\text{Si}_2\text{H}_6$ . The carbon number in particular of the hydrocarbon group which replaces the hydrogen atom of these Silang system compound is not limited. Although based also on the number of substitution, it is expectable that film density falls [ the one where a carbon number is to some extent larger ] according to increase of the steric exclusion of a hydrocarbon group as a general tendency, and specific inductive capacity falls, and the mobility of the membrane formation intermediate in a film growth process improves. The carbon content of the dielectric film which will be obtained on the other hand if a carbon number is not much large increases, moisture resistance deteriorates, satisfying membranous quality becomes not easily obtained by plasma CVD, either, and also it becomes difficult to deal with an organic silane compound as a gas. Therefore, as a hydrocarbon group which replaces the hydrogen atom of the Silang system compound, allyl groups, such as alkyl groups of 1-2 carbon numbers, such as a methyl group and an ethyl group, or a phenyl group, are suitable. On the other hand, as the above-mentioned oxidizer, oxygen ( $\text{O}_2$ ), ozone ( $\text{O}_3$ ), hydrogen peroxide ( $\text{H}_2\text{O}_2$ ), etc. can be used.

[0016] In particular, it is organicity. It is a monomethyl silane as a silane compound.  $[\text{Si}(\text{CH}_3)_3 \text{H}]$  When  $\text{H}_2\text{O}_2$  is used as an oxidizer, the dielectric film of the form where carbon was incorporated into the  $\text{SiO}_2$  film of the stoichiometric composition acquired by the thermal oxidation of silicon can be obtained. The applicant for this patent has found out that the mobility of a membrane formation intermediate improves about this  $\text{Si}(\text{CH}_3)$



$H_3/H_2O_2$  system when forming temperature is 20 °C or less in LPCVD before. It has been thought that it is inferior to membraneous quality while the dielectric film containing the carbon formed by the above systems of reaction is more advantageous to lower-dielectric-constant-izing than before. However, if membrane formation which switched plasma CVD and LPCVD like this invention is performed, even if it is such the system of reaction, good membraneous quality and lower dielectric constant can be reconciled.

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## EXAMPLE

[Example]Hereafter, the concrete example of this invention is described.

[0018]Example 1 -- here, this invention being applied to formation of the interlayer insulation film in a semiconductor wafer process, and, By performing the plasma CVD and LPCVD by an  $\text{Si}(\text{CH}_3)_2\text{H}_2/\text{H}_2\text{O}_2$  system continuously, the  $\text{SiO}_x$  system interlayer insulation film of two-layer composition with low specific inductive capacity was formed. This example of a process is explained referring to drawing 1 and drawing 2. The device used by this example is connected common to one set of the object for plasma CVD, the object for LPCVD, and the wafer handling unit by which each of the chamber for post annealing was maintained by the predetermined degree of vacuum, It is the multi chamber-type device made as [ perform / conveyance of the base between each chamber / altogether / via this wafer handling unit ].

[0019]The wafer W in which 0.65-micrometer-high aluminum system circuit pattern 2 was first formed [ on the substrate 1 ] according to the line and space which is 0.4 micrometer as a metal wiring pattern beforehand was prepared. Among the above-mentioned substrate 1, although a field corresponding directly under aluminum system circuit pattern 2 comprises an insulator layer, the structure under the common metallic wiring of the usual semiconductor device is not illustrated here.

[0020]Next, this wafer W was carried in to the plasma CVD device, and plasma CVD was performed on condition of the following as an example.

$\text{Si}(\text{CH}_3)_2\text{H}_2$  flow 100 SCCM Ar flow 500 SCCM  $\text{H}_2\text{O}_2$  (gas) speed of supply A part for 0.7 g/ Pressure 160 Pa RF power 200 W (13.56 MHz)

1st  $\text{SiO}_x$  film 3<sub>p</sub> with a thickness of about 0.1 micrometer which covers aluminum system circuit pattern 2 to conformal one mostly as it can wafer-temperature 350 °C. Come, and is alike and it is shown more in drawing 1 (it means that the subscript P relates to a plasma process.) It is the same as that of the following. Membranes were formed. The specific inductive capacity of this 1st  $\text{SiO}_x$  film 3<sub>p</sub> was a little lower than the specific inductive capacity  $\epsilon_{\text{film}} = 3.9$  of the  $\text{SiO}_2$  film of the stoichiometric composition acquired by the thermal oxidation of silicon. This is an effect of the methyl group incorporated into the film.

[0021]Next, the above-mentioned wafer W was conveyed to the LPCVD device under the high vacuum, and LPCVD was performed on condition of the following as an example.

$\text{Si}(\text{CH}_3)_2\text{H}_2$  flow 100 SCCM Ar flow 500 SCCM  $\text{H}_2\text{O}_2$  (gas) speed of supply a part for 0.7g/- pressure 133 Pa wafer temperature 0 °C -- thereby, It is 2nd  $\text{SiO}_x$  film 4<sub>L</sub> (it means that the subscript L relates to a LPCVD

process.) about 0.1 micrometer thick so that the surface step of the base resulting from aluminum system circuit pattern 2 may be canceled mostly, as shown in drawing 2. It is the same as that of the following. Membranes were formed. The specific inductive capacity of this 2nd  $\text{SiO}_x$  film 4<sub>L</sub> was still lower than the dielectric constant of

the above-mentioned 1st SiOx film 3<sub>p</sub>.

[0022]Then, the chamber for post annealing was conveyed for the wafer W, 400 °C and post annealing for 15 minutes were performed among N<sub>2</sub> atmosphere of 1.01x10<sup>5</sup>Pa, and the moisture which remains in the film of 2nd SiOx film 4<sub>L</sub> was removed. The specific inductive capacity epsilon of the interlayer insulation film 5 measured in this stage, i.e., the film which doubled the above-mentioned 1st SiOx film 3<sub>p</sub> and 2nd SiOx film 4<sub>L</sub>, was about 3.2. Although the acceleration deterioration test of 1000 hours under the relative humidity of 100%, the temperature of 120 °C, and humid high-temperature-high-pressure environment with a pressure of 2 atmospheres was done to the base of this state, neither the corrosion of aluminum system circuit pattern 2 nor degradation of hot carrier tolerance was accepted at all. Therefore, it was proved that the above-mentioned interlayer insulation film 5 had specific inductive capacity low as a whole, and was excellent also in moisture resistance.

[0023]In example 2 this example, surface treatment processing by oxygen plasma was performed to 2nd SiOx film 4<sub>L</sub> formed in Example 1. Here the used device between each chamber the object for plasma CVD, the object for LPCVD, for plasma treatment, and for post annealing, it is the multi chamber-type device made as [perform / conveyance of the base between each chamber / it is connected to the wafer handling unit by which the base was maintained at the high vacuum, and / altogether / via this wafer handling unit ].

[0024]The stage film formation of the above-mentioned 2nd SiOx film 4<sub>L</sub> is as having mentioned above in Example 1. In this example, the following conditions performed oxygen plasma treatment as opposed to this film continuously.

O<sub>2</sub> flow 2000 SCCM Ar flow 1000 SCCM Pressure 133 Pa RF power 500 W (13.56 MHz)

wafer temperature 350 °C processing time a part for three -- of this plasma treatment, by the layer part of 2nd SiOx film 4<sub>L</sub>, etubation of drying and a film advanced and reforming layer 6<sub>p</sub> as shown in drawing 3 was formed.

Since the wafer temperature at the time of the above-mentioned plasma treatment is the same as the wafer temperature at the time of membrane formation of 1st SiOx film 3<sub>p</sub> by the above-mentioned plasma CVD, it can be considered as the chamber for plasma CVD, and common use, without providing the above-mentioned chamber for plasma treatment separately, and can also respond by the change of the gas supplied to a chamber, RF power, and an exhaust speed.

[0025]Then, the same post annealing as Example 1 was performed to the above-mentioned wafer W. In this example, the interlayer insulation film 7 which consists of three persons of 1st SiOx film 3<sub>p</sub>, 2nd SiOx film 4<sub>L</sub>, and reforming layer 6<sub>p</sub> was formed. The specific inductive capacity epsilon as this whole interlayer insulation film 7 was about 3.3. Since the rise of the specific inductive capacity by the densification of reforming layer 6<sub>p</sub>

influenced, it is thought of that the specific inductive capacity epsilon became a little higher than Example 1. The result of the acceleration deterioration test of this interlayer insulation film 7 was better than Example 1.

[0026]In example 3 this example, after performing even formation of reforming layer 6<sub>p</sub> like above-mentioned Example 2, the 3rd dielectric film by plasma CVD was further laminated on this. That is, the wafer W of the state which showed in drawing 3 shown above was again returned to the plasma CVD device used for membrane formation of 1st SiOx film 3<sub>p</sub>, and plasma CVD was performed on condition of the following as an example.

Si(CH<sub>3</sub>)<sub>2</sub> H<sub>2</sub> flow 80 SCCM Ar flow 500 SCCM H<sub>2</sub>O<sub>2</sub> (gas) speed of supply a part for 0.85g/s -- pressure 93 Pa wafer temperature 350 °C -- thereby, 3rd SiOx film 8<sub>p</sub> as shown in drawing 4 was formed at the thickness which is about 0.3 micrometer.

[0027]Then, the same post annealing as Example 1 was performed to the above-mentioned wafer W. In this

example, the interlayer insulation film 9 which consists of four persons of 1st SiOx film 3<sub>p</sub>, 2nd SiOx film 4<sub>L</sub>, reforming layer 6<sub>p</sub>, and 3rd SiOx film 8<sub>p</sub> was formed. The specific inductive capacity epsilon as this whole interlayer insulation film 9 was about 3.6. It is because 3rd SiOx film 8<sub>p</sub> with membraneous quality there are few carbon contents and precise [ that this specific inductive capacity epsilon rose further rather than Example 2 ] and high specific inductive capacity was added. The result of the acceleration deterioration test of this interlayer insulation film 9 was still better than Example 2.

[0028]As mentioned above, although this invention was explained based on the example of three examples, this invention is not limited to these examples at all, and change, selection, and combination are possible for it suitably about details, such as composition of a sample wafer, a size of each part, a film formation condition, plasma treatment conditions, and a post annealing condition.

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DESCRIPTION OF DRAWINGS

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## [Brief Description of the Drawings]

[Drawing 1]In the example of a process which applied this invention to formation of the interlayer insulation film of a semiconductor device, it is a typical sectional view showing the state where covered aluminum system circuit pattern formed on the substrate, and the 1st SiOx film by plasma CVD was formed.

[Drawing 2]It is a typical sectional view showing the state where formed the 2nd SiOx film by LPCVD on the 1st SiOx film of drawing 1, and flattening of the wafer surface was carried out mostly.

[Drawing 3]It is a typical sectional view showing the state where the surface of the 2nd SiOx film of drawing 2 was reformed by oxygen plasma treatment.

[Drawing 4]It is a typical sectional view showing the state where the 3rd SiOx film was further formed by plasma CVD on the 2nd SiOx film of drawing 3.

## [Description of Notations]

1 -- Substrate 2 -- aluminum system circuit pattern 3 <sub>P</sub> -- The 1st SiOx film 4 <sub>L</sub> -- The 2nd SiOx film 5, 7, 9 -- Interlayer insulation film 6 <sub>P</sub> -- Reforming layer 8 <sub>P</sub> -- The 3rd SiOx film W -- Wafer

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[Translation done.]

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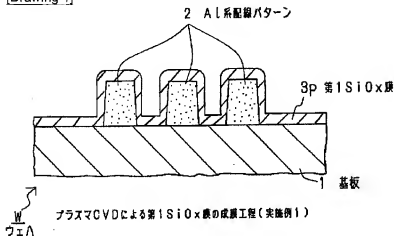
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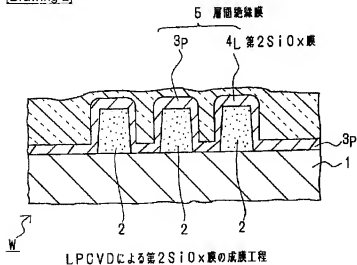
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## DRAWINGS

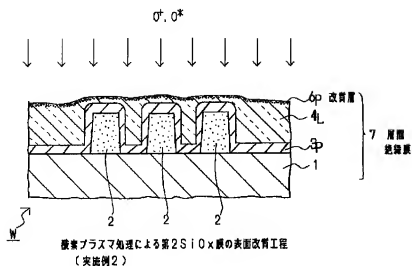
[Drawing 1]



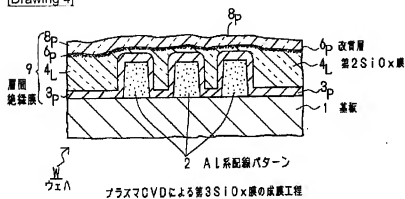
[Drawing 2]



[Drawing 3]



[Drawing 4]



[Translation done.]

# PATENT ABSTRACTS OF JAPAN

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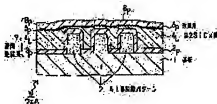
(72)Inventor : HARA MASATERU

## (54) FORMATION OF SILICON OXIDE DIELECTRIC FILM

(57)Abstract:

**PROBLEM TO BE SOLVED:** To provide a silicon oxide dielectric film which can be used as an interlayer insulating film in a semiconductor device and can realize both a low dielectric constant and a long-term reliability.

**SOLUTION:** With use of a monomethyl silane/hydrogen peroxide film-forming gas, a first moisture-resistive SiOx film 3P is formed directly on an Al-based wiring pattern 2 by a plasma CVD process, and a second SiOx film 4L having a high fluidity for reducing a step difference on a surface of a wafer W is formed on the film 3P by a low-temperature, low-pressure (LPCVD) process. A modified layer 6P may be formed by an oxygen plasma modification process on the second SiOx film 4L, and further a third SiOx film 8P may be formed on the modified layer 6P by the plasma CVD process with use of the same film-forming gas as the above. Any of the SiOx films 3P, 4L and 8P is lower in relative permittivity than a silicon oxide film of a stoichiometric composition obtained by thermally oxidizing silicon, and thus the overall relative permittivity of an interlayer insulating film 9 can be kept low.





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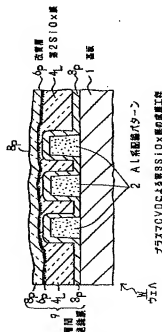
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(54) 【発明の名称】 酸化シリコン系誘電体膜の形成方法

(57) 【要約】

【課題】 半導体デバイスの層間絶縁膜として用いられる酸化シリコン系誘電体膜の低誘電率化と長期信頼性とを両立させる。

【解決手段】 モノメチルシラン／過酸化水素系の成膜ガスを使用し、A I 系配線パターン2を直接被覆する耐湿性に優れた第1 SiO<sub>2</sub>膜3pはプラズマCVDで、その上を被覆してウェハWの表面段差を緩和する流動性の高い第2 SiO<sub>2</sub>膜4Lは低温のLPCVDで成膜する。第2 SiO<sub>2</sub>膜4Lの表面には酸素プラズマ改質処理で改質層6pを形成しても良く、さらにその上に上記と同じ成膜ガス系によるプラズマCVDで第3 SiO<sub>2</sub>膜8pを形成しても良い。いずれのSiO<sub>2</sub>膜3p、4L、8pもシリコンを熱酸化して得られる化学量論的組成の酸化シリコン膜よりも比誘電率が低く、したがって、層間絶縁膜9全体としての比誘電率を低く維持することができる。



## 【特許請求の範囲】

【請求項1】 シリコンを熱酸化して得られる化学量論的組成の酸化シリコン膜よりも比誘電率の低い第1誘電体膜を、基板上の金属配線パターンを被覆することくプラズマCVDにより成膜する第1工程と、

前記プラズマCVDで用いた成膜ガスと同一成分からなる成膜ガスを用いて減圧CVDを行うことにより、前記第1誘電体膜よりさらに比誘電率の低い第2誘電体膜を、該第1誘電体膜上に基体の表面段差を緩和することく成膜する第2工程とを有することを特徴とする酸化シリコン系誘電体膜の形成方法。

【請求項2】 前記成膜ガスとして、フッ素を構成元素とするガス成分を含まないものを用いることを特徴とする請求項1記載の酸化シリコン系誘電体膜の形成方法。

【請求項3】 前記第2誘電体膜を成膜後、その表面を硬化させるためのプラズマ改質処理を施すことを特徴とする請求項1記載の酸化シリコン系誘電体膜の形成方法。

【請求項4】 前記第2誘電体膜を成膜後、前記プラズマCVDで用いた成膜ガスと同一成分からなる成膜ガスを用いて再度プラズマCVDを行うことにより、シリコンを熱酸化して得られる熱酸化シリコン膜よりも比誘電率の低い第3誘電体膜を該第2誘電体膜上に成膜することを特徴とする請求項1記載の酸化シリコン系誘電体膜の形成方法。

【請求項5】 前記第2誘電体膜を成膜後、その表面を硬化させるためのプラズマ改質処理を施し、しかる後に前記プラズマCVDで用いた成膜ガスと同一成分からなる成膜ガスを用いて再度プラズマCVDを行うことにより、シリコンを熱酸化して得られる化学量論的組成の酸化シリコン膜よりも比誘電率の低い第3誘電体膜を該第2誘電体膜上に成膜することを特徴とする請求項1記載の酸化シリコン系誘電体膜の形成方法。

【請求項6】 前記第1誘電体膜を成膜するためのプラズマCVDの成膜ガスとして、シラン系化合物の水素原子の少なくとも1個が炭化水素基に置換された有機シラン化合物と酸化剤とを含むガスを用いることを特徴とする請求項1記載の酸化シリコン系誘電体膜の形成方法。

【請求項7】 前記有機シラン化合物としてモノメチルシラン、前記酸化剤として過酸化水素を用いることを特徴とする請求項6記載の酸化シリコン系誘電体膜の形成方法。

## 【発明の詳細な説明】

## 【0001】

【発明の属する技術分野】 本発明はたとえば半導体デバイスの層間絶縁膜として用いられる誘電体膜の形成方法に関し、特に該の低誘電率化と長期信頼性とを両立させる方法に関する。

## 【0002】

【従来の技術】 近年の半導体デバイス製造においては、

その高集積化、高機能化に伴い、基板上に層間絶縁膜を介して金属配線パターンを層間にも積み上げる多層配線技術の採用が必須となっている。多層配線を採用する場合、デザイン・ルールとの縮小と共に隣接配線同士あるいは上下配線同士が接近してくると、比誘電率 $\epsilon$ が約3.9と大きい従来の $\text{SiO}_2$ 系層間絶縁膜では、配線間容量が大きくなり過ぎる。そこで、特にデザイン・ルール0.25 $\mu\text{m}$ 以降の世代では、比誘電率の低い誘電体膜（以下、低誘電体膜と称する。）を用いて低電圧駆動、低消費電力、高クロック周波数を実現することが検討されている。

【0003】 低誘電体膜としては、これまでに有機系低誘電体膜と無機系低誘電体膜とが検討されている。そもそも $\text{SiO}_2$ の比誘電率 $\epsilon$ が約3.9と大きいのは、 $\text{SiO}_2$ の骨格をなすシリキサン（ $-\text{Si}-\text{O}-$ ）結合中のO原子の電気陰性度が大きいために電子がO原子側に偏っており、電場が与えられるとその偏りが一層増大するからである。したがって、低誘電率化には分極率の低下が不可欠である。その点、有機系低誘電体膜では立体障害の大きいアルキル基が存在するおかげで膜の密度と分子そのものの分極率が低下しており、これにより比誘電率の低下がもたらされている。たとえば、ポリイミド系樹脂膜で比誘電率 $\epsilon=3.5\sim3.0$ 、フッ素系樹脂膜で $\epsilon=2.7\sim1.9$ の値が達成されている。

【0004】 一方、無機系低誘電体膜としては、プラズマCVDにより成膜可能な $\text{SiOF}$ 膜、すなわちF（フッ素）を含有する $\text{SiO}_x\text{F}_y$ 膜が主として検討されている。 $\text{SiOF}$ 膜の比誘電率は膜中のF濃度の増加に伴って減少し、これまでに3.7 $\sim$ 3.2程度の値が達成されている。 $\text{SiO}_x$ の比誘電率がFを含有することにより低下する理由は、まだ十分に解明されていないが、電子雲の歪みに起因する電子分極と、核変位に起因するイオン分極の両方が減少するためと考えられている。

## 【0005】

【発明が解決しようとする課題】 しかしながら、上述の有機系低誘電体膜も無機系誘電体膜も、それぞれに問題を抱えている。まず、有機系低誘電体膜の中には、溶剤に溶解させたポリマー材料を基体上にスピンコートした後、この塗膜を加熱して脱水重合させることにより形成されるものも多い。このような膜では、重合時に生成した水や溶剤が膜中に取り込まれやすく、これらの水や溶剤が金属配線パターンを腐食させる原因となる。ポリマー重合をラジカル重合で達成できれば水や溶剤の問題は生じないため、プラズマCVDで成膜できるフッ素化アルモルファス・カーボン膜等の膜も提案されている。しかし、有機膜は分子骨格の基本が炭素鎖であるために酸素プラズマ耐性に本質的に劣り、コンタクト・ホール開口後のレジスト・アッシング時に膜減りを起こすことが問題となっている。

【0006】 一方、無機系低誘電体膜の代表例であるS

SiO<sub>2</sub>膜には、大気放置中に急速に吸湿し、膜自身あるいはプロセスの安定性を劣化させるという問題がある。これは、吸湿により生じたフッ酸(HF)が、金属配線パターンを腐食させるのみならず、半導体製造装置を汚染・腐食させたり、あるいは層間絶縁膜の平坦化をCMP(化学機械研磨)により行う場合の研磨スラリーのpHを変化させ、結果的に研磨速度を変動させるからである。吸湿性の高い膜では、1個のSi原子に2個のF原子が結合したと考えられるSi(-F)<sub>2</sub>結合、O原子を介して近接したものと考えられるSi-F結合が存在しており、これらの結合が加水分解反応を経てSi-OH結合に変化し、このSi-OH結合が大気中のH<sub>2</sub>Oとの間で水素結合を形成することにより吸湿が進行すると考えられている。

【0007】したがって、有機系低誘電率膜も無機系低誘電率膜も、単独で層間絶縁膜として使用することは現状では極めて難しい。このため、流動性に優れた低誘電率膜の上下を、比誘電率がやや高いが膜質に比較的優れたSiO<sub>2</sub>膜やSi<sub>3</sub>N<sub>4</sub>膜で挟んだ複合膜構成の層間絶縁膜が提案されている。たとえば、1995年ドライ・プロセス・シンポジウム抄録集p. 261~268には、Al配線パターンを被覆する層間絶縁膜を下層側から順にペース層、フロー層、キャップ層の3層構成とし、ペース層とキャップ層はSiH<sub>4</sub>/N<sub>2</sub>O/N<sub>2</sub>混合ガス系を用い、基板温度300℃のプラズマCVDで、またフロー層はSiH<sub>4</sub>/H<sub>2</sub>O<sub>2</sub>/N<sub>2</sub>系を用い、基板温度0℃の減圧CVD(LPCVD)でそれぞれ成膜する方法が提案されている。また、月刊セミコンダクターワールド1996年2月号p. 86~88(プレスジャーナル社刊)には、Al配線パターンを被覆する層間絶縁膜を下層から順にバリヤ膜、SiO<sub>2</sub>膜、バリヤ膜の3層構成とし、該バリヤ膜としてSiO<sub>2</sub>膜を用いる方法が記載されている。その他、塗布型の有機系低誘電率膜の上下を膜質に比較的優れたSiO<sub>2</sub>膜やSi<sub>3</sub>N<sub>4</sub>膜で挟むことも、広く知られている。

【0008】しかしながら、これらの複合膜形成技術では上記ペース層、キャップ層、バリヤ層を構成する材料がいずれも比誘電率の高いSiO<sub>2</sub>膜、あるいはこれよりさらに比誘電率の高いSi<sub>3</sub>N<sub>4</sub>膜であり、層間絶縁膜全体としての比誘電率の低下に限界が生じている。また、膜中に水分を含む流動性の高い膜の上下を水分の少ない膜で挟む場合、上層側の膜については水分を上側へ透過させる機能、下層側の膜についてはその下側の金属配線パターンを保護するために水分を下側へ透過させない特性が要求され、最適な膜種の選択が困難であるという問題があった。そこで本発明は、この吸湿性の問題を解決し、低誘電率化を図ると共に長期信頼性にも優れた誘電率膜を形成する方法を提供することを目的とする。

【0009】

【課題を解決するための手段】本発明の酸化シリコン系

誘電率膜の形成方法では、基体上の金属配線パターンに直接的に接する部分に膜質の良い膜を配し、その上を比誘電率が低く流動性の高い膜で被覆して基体の平坦化を図るという従来の考え方を踏襲しつつも、個々の膜としてはいずれもシリコンを熱酸化して得られる化学量論的組成の酸化シリコン膜よりも比誘電率の低いものを用いて層間絶縁膜全体の誘電率を低く維持し、しかも個々の膜を同一成分からなる成膜ガスを用いて異なるCVD条件、すなわちプラズマCVDとLPCVDで成膜し分けるという簡易な手法を採ることにより、上述の目的を達成するものである。すなわち、金属配線パターンを被覆する第1誘電率膜をプラズマCVDで成膜した後、その上に基体の表面段差を緩和する第2誘電率膜をLPCVDで成膜する。

【0010】本発明では、フッ素を構成元素とするガス成分を含む成膜ガスは使用しない。つまり、本発明により形成される酸化シリコン系誘電率膜は、SiO<sub>2</sub>膜のように膜中へフッ素原子を取り込むことによる低誘電率化を期待するものではない。第2誘電率膜を成膜した後には、その表面を硬化させるためのプラズマ改質処理を施しても良いし、あるいは先のプラズマCVDで用いた成膜ガスと同一成分からなる成膜ガスを用いて再度プラズマCVDを行うことにより、さらに第3誘電率膜を積層しても良い。この第3誘電率膜も当然、シリコンを熱酸化して得られる化学量論的組成の酸化シリコン膜よりも比誘電率の低いものである。さらには、第2誘電率膜の表面のプラズマ改質処理と、その上への第3誘電率膜の積層の両方を行っても良い。

【0011】

【発明の実施の形態】本発明は、同一成分からなる成膜ガスを用いてもCVD条件により誘電率膜の膜質が変化することに着目し、簡易で制御性の高い誘電率膜の形成を実現しようとするものである。プラズマCVDでは膜に対してイオン・スパッタ作用が働くため膜の密度が上昇するため、大幅な低誘電率化は望めない。しかしその一方で、膜形成が本質的にラジカル重合反応にもとづいていること、およびイオン・スパッタ作用による脱水効果が期待できることにより、水分含有量が極めて少なく、緻密な膜質を有する誘電率膜を形成することができ、この膜は、金属配線パターンを最初に被覆しこれを保護する第1誘電率膜、あるいは層間絶縁膜の最上層を被覆してパッシベーションの役割を果たす第3誘電率膜として好都合である。この第1誘電率膜と第3誘電率膜の比誘電率は、シリコンを熱酸化して得られる化学量論的組成の酸化シリコン膜の比誘電率(約3.9)よりも低いので、従来のように低誘電率膜の上下をSiO<sub>2</sub>膜で挟む場合に比する層間絶縁膜全体としての比誘電率を下げることも可能である。

【0012】一方、LPCVD法ではイオン・スパッタ作用のような物理的作用が膜に働くがない、膜表面にお

ける成膜種のマイグレーションが促進されるので、カバレッジの良い誘電体膜を形成することができ、しかも膜の密度がそれほど高くならないので比誘電率を下げることができる。この膜は、金属配線パターンに起因する基体の表面段差を緩和しながら、層間絶縁膜全体の比誘電率の実質的な低下に寄与する第2誘電体膜として好都合である。

【0013】本発明では、上述のようなプラズマCVDとLPCVDとが同一成分からなる成膜ガスを用いて行われるので、成膜される第1誘電体膜と第2誘電体膜、あるいは必要に応じて追加される第3誘電体膜は、成膜条件による元素組成比の若干の違いはあるものの、化学組成は基本的に共通である。したがって、化学組成の全く異なる異種の膜を積層する場合と異なり、膜種の選択に困難を来すこともなくなる。

【0014】本発明において第1誘電体膜と第2誘電体膜、あるいは必要に応じて第3誘電体膜を成膜する場合、フッ素(F)を構成元素とするガス成分を含まない成膜ガスを使用すると、膜からFを排除することができる。したがって、膜の吸湿によるフッ酸(HF)の生成、これによる金属配線パターンの腐食、CMPにおける研磨速度のパラツキといった問題をすべて回避することができる。なお、上記のプラズマCVDとLPCVDとは、基体を途中で長時間にわたって大気開放することなく、連続的に行うことが好適である。ただし、これら両CVDの成膜温度が大きく異なり、しかも基体の加熱を該基体を載置するステージの温度制御により行っている場合には、同一チャンバで両CVDを連続して行おうとすると、ステージの温調に伴う時間のロスが大きくなる。したがってこのような場合には、予めステージ温度設定の異なるプラズマCVDチャンバとLPCVDチャンバとを真空搬送路で接続したマルチャンバ型の装置を使用することが好適である。

【0015】第1誘電体膜、あるいは必要に応じて追加される第3誘電体膜を成膜するためのプラズマCVD用成膜ガスとしては、シラン系化合物の水素原子の少なくとも1個が炭化水素基に置換された有機シラン化合物と酸化剤とを含むガスを用いることが好適である。上記有機シラン化合物の基本骨格は、モノシラン $\text{SiH}_4$ であっても、あるいはジシラン $\text{Si}_2\text{H}_6$ 等のポリシランであっても良い。これらシラン系化合物の水素原子を置換する炭化水素基の炭素数は特に限定されるものではない。置換数にもよるが、一般的な傾向としては、炭素数がある程度大きい方が炭化水素基の立体障害の増大により膜密度が低下して比誘電率が下がり、また膜成長過程における成膜中間体の流動性が向上することが期待できる。反面、炭素数が多いと得られる誘電体膜の炭素含有量が増大して耐湿性が劣化し、プラズマCVDに

よっても満足ゆく膜質が得られにくくなる他、有機シラン化合物を気体として取り扱うことが困難となる。したがって、シラン系化合物の水素原子を置換する炭化水素基としては、メチル基やエチル基等、炭素数1〜2個のアルキル基、あるいはフェニル基等のアール基が適当である。一方、上記酸化剤としては、酸素( $\text{O}_2$ )、オゾン( $\text{O}_3$ )、過酸化水素( $\text{H}_2\text{O}_2$ )等を用いることができる。

【0016】特に、有機シラン化合物としてモノメチルシラン $[\text{Si}(\text{CH}_3)_2\text{H}_2]$ 、酸化剤として $\text{H}_2\text{O}_2$ を使用した場合には、シリコンの熱酸化により得られる化学量論的組成の $\text{SiO}_2$ 膜に炭素が取り込まれた形の誘電体膜を得ることができる。この、 $\text{Si}(\text{CH}_3)_2\text{H}_2/\text{H}_2\text{O}_2$ 系に関しては、LPCVDにおいて成膜温度を $20^\circ\text{C}$ 以下とした場合に成膜中間体の流動性が向上することを、本発明出人が以前に見出して、上記のような反応系により成膜される炭素を含む誘電体膜は、従来より低誘電率化に有利な一方で膜質には劣るものと考えられてきた。しかし、本発明のようにプラズマCVDとLPCVDを切り換えた成膜を行えば、このような反応系であっても良好な膜質と低誘電率とを両立させることができる。

【0017】

【実施例】以下、本発明の具体的な実施例について説明する。

#### 【0018】実施例1

ここでは、本発明を半導体ウェハ・プロセスにおける層間絶縁膜の形成に適用し、 $\text{Si}(\text{CH}_3)_2\text{H}_2/\text{H}_2\text{O}_2$ 系によるプラズマCVDとLPCVDとを連続して行うことにより、比誘電率の低い2層構成の $\text{SiO}_x$ 系層間絶縁膜を形成した。このプロセス例について、図1および図2を参照しながら説明する。本実施例で用いた装置は、プラズマCVD用、LPCVD用、およびポストアニール用のチャンバの各々が所定の真空度に維持された1基のウェハ・ハンドリング・ユニットに共通に接続され、各チャンバ間での基体の搬送がすべてこのウェハ・ハンドリング・ユニットを介して行われるようになされたマルチャンバ型の装置である。

【0019】まず基板1上に予め金属配線パターンとして高さ0.65 $\mu\text{m}$ のA1系配線パターン2を、4.5 $\mu\text{m}$ のライン・アンド・スペースにしたがって形成されたウェハWを準備した。上記基板1中、A1系配線パターン2の直下に相当する領域は絶縁膜にて構成されるが、ここでは通常の半導体デバイスの一般的な金属配線下の構造は図示しない。

【0020】次に、このウェハWをプラズマCVD装置に搬入し、一例として下記の条件でプラズマCVDを行った。

$\text{Si}(\text{CH}_3)_2\text{H}_2$ 流量	100 SCCM
Ar 流量	500 SCCM

H <sub>2</sub> O <sub>2</sub> (気体) 供給速度	0.7 g/分
圧力	160 Pa
RFパワー	200 W (13.56 MHz)
ウェハ温度	350 °C

これにより、図1に示されるように、A1系配線パターン2をほぼコンフォーマルに被覆する厚さ約0.1 μmの第1 SiO<sub>2</sub>膜3p (添字Pは、プラズマ・プロセスに関連することを表す。以下同様。) が成膜された。この第1 SiO<sub>2</sub>膜3pの比誘電率は、シリコンの熱酸化で得られる化学量論的組成のSiO<sub>2</sub>膜の比誘電率ε = 3.9よりも若干低かった。これは、膜中に取り込まれたメチル基の効果である。

【0021】次に、上記のウェハWを高真空中にてLPCVD装置へ搬送し、一例として下記の条件でLPCVDを行った。

Si (CH <sub>3</sub> ) H <sub>3</sub> 流量	100 SCCM
Ar 流量	500 SCCM
H <sub>2</sub> O <sub>2</sub> (気体) 供給速度	0.7 g/分
圧力	133 Pa
ウェハ温度	0 °C

これにより、図2に示されるように、A1系配線パターン2に起因する基体の表面凹凸をほぼ解消するように厚さ約0.1 μmの第2 SiO<sub>2</sub>膜4L (添字Lは、LPCVDプロセスに関連することを表す。以下同様。) が成膜された。この第2 SiO<sub>2</sub>膜4Lの比誘電率は、上記第1 SiO<sub>2</sub>膜3pの誘電率よりもさらに低かった。

【0022】この後、ウェハWをポストアニール用チャンバへ搬送し、1.01 × 10<sup>5</sup> PaのN<sub>2</sub> 雰囲気中、

O <sub>2</sub> 流量	2000 SCCM
Ar 流量	1000 SCCM
圧力	133 Pa
RFパワー	500 W (13.56 MHz)
ウェハ温度	350 °C
処理時間	3 分

このプラズマ処理により、第2 SiO<sub>2</sub>膜4Lの表層部では脱水と膜の緻密化が進行し、図3に示されるような改質層6pが形成された。なお、上記プラズマ処理時のウェハ温度は前述のプラズマCVDによる第1 SiO<sub>2</sub>膜3pの成膜時のウェハ温度と同じなので、上記プラズマ処理用チャンバを別個に設けずにプラズマCVD用チャンバと共用とし、チャンバへ供給するガス、RFパワー、排気速度の切替えで対応することもできる。

【0025】この後、上記ウェハWに対して実施例1と同様のポストアニールを行った。本実施例では、第1 SiO<sub>2</sub>膜3p、第2 SiO<sub>2</sub>膜4L、および改質層6pの三者からなる層間絶縁膜7が形成された。この層間絶縁膜7の全体としての比誘電率εは、約3.3であった。比誘電率εが実施例1よりもやや高くなったのは、改質層6pの高密度化による比誘電率の上昇が影響したためと考えられる。なお、この層間絶縁膜7の加速劣化試

400 °C、15分間のポストアニールを行い、第2 SiO<sub>2</sub>膜4Lの膜中に残存する水分を除去した。この段階で測定した層間絶縁膜5、すなわち上記第1 SiO<sub>2</sub>膜3pと第2 SiO<sub>2</sub>膜4Lとを合わせた膜の比誘電率εは、約3.2であった。また、この状態の基体に対して相対湿度100%、温度120 °C、圧力2気圧の湿潤高温環境下における1000時間の加速劣化試験を行ったが、A1系配線パターン2の腐食やホットキャリア耐性の劣化は何ら認められなかった。したがって、上記層間絶縁膜5が全体として低い比誘電率を有し、耐湿性にも優れていることが実証された。

#### 【0023】実施例2

本実施例では、実施例1で成膜された第2 SiO<sub>2</sub>膜4Lに、酸素プラズマによる表面改質処理を施した。ここで用いた装置は、プラズマCVD用、LPCVD用、プラズマ処理用、およびポストアニール用の各チャンバ間で、基体が高真空中に維持されたウェハ・ハンドリング・ユニットに接続され、各チャンバ間で基体の搬送がすべてこのウェハ・ハンドリング・ユニットを介して行われるようになされたマルチチャンバ式の装置である。

【0024】上記第2 SiO<sub>2</sub>膜4Lの成膜工程までは、実施例1で上述したとおりである。本実施例では続いてこの膜に対し、たとえば下記のような条件で酸素プラズマ処理を行った。

試験の結果は、実施例1よりも良好であった。

#### 【0026】実施例3

本実施例では、改質層6pの形成までを上述の実施例2と同様に行った後、さらにこの上にプラズマCVDによる第3の誘電体膜を積層した。すなわち、前掲の図3に示した状態のウェハWを第1 SiO<sub>2</sub>膜3pの成膜に用いたプラズマCVD装置に再び戻し、一例として下記の条件でプラズマCVDを行った。

Si (CH <sub>3</sub> ) H <sub>3</sub> 流量	80 SCCM
Ar 流量	500 SCCM
H <sub>2</sub> O <sub>2</sub> (気体) 供給速度	0.85 g/分
圧力	93 Pa
ウェハ温度	350 °C

これにより、図4に示されるような第3 SiO<sub>2</sub>膜8pが約0.3 μmの厚さに成膜された。

【0027】この後、上記ウェハWに対して実施例1と

同様のポストアニールを行った。本実施例では、第1 SiO<sub>2</sub>膜3p、第2 SiO<sub>2</sub>膜4L、改質層6p、および第3 SiO<sub>2</sub>膜8pの四者からなる層間絶縁膜9が形成された。この層間絶縁膜9の全体としての比誘電率εは、約3.6であった。この比誘電率εが実施例2よりもさらに上昇したのは、炭素含有量が少なく膜質が緻密で比誘電率の高い第3 SiO<sub>2</sub>膜8pが追加されたからである。なお、この層間絶縁膜9の加速劣化試験の結果は、実施例2よりもさらに良好であった。

【0028】以上、本発明を3例の実施例にもとづいて説明したが、本発明はこれらの実施例に何ら限定されるものではなく、サンプル・ウェハの構成、各部の寸法、成膜条件、プラズマ処理条件、ポストアニール条件等の細部については適宜変更、選択、組合せが可能である。

【0029】

【発明の効果】以上の説明からも明らかなように、本発明によれば、低誘電率化には有利でも高膜質化を望むことは難しかった従来の反応系も、成膜条件次第で優れた膜質を有する誘電体膜の成膜に適用することが可能となる。したがって、低誘電体膜の上下をSiO<sub>2</sub>膜やSiN膜のように比誘電率の高い膜で挟み込むことなく、シリコンの熱酸化で得られる化学量論的組成のSiO<sub>2</sub>膜よりも比誘電率の小さい膜のみを用いて誘電体膜を構成

することができる。本発明を半導体デバイスの製造プロセスにおける層間絶縁膜の成膜に適用した場合には、該層間絶縁膜の低誘電率化と長期信頼性の向上とが両立され、このことによって半導体デバイスの高集積化や動作高速化を実現する上での障害が克服される。

【図面の簡単な説明】

【図1】本発明を半導体デバイスの層間絶縁膜の形成に適用したプロセス例において、基板上に形成されたAl系配線パターンを被覆してプラズマCVDによる第1 SiO<sub>2</sub>膜を成膜した状態を示す模式的断面図である。

【図2】図1の第1 SiO<sub>2</sub>膜上にLPCVDにより第2 SiO<sub>2</sub>膜を成膜し、ウェハ表面をほぼ平坦化した状態を示す模式的断面図である。

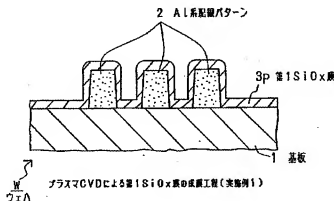
【図3】図2の第2 SiO<sub>2</sub>膜の表面を酸素プラズマ処理により改質した状態を示す模式的断面図である。

【図4】図3の第2 SiO<sub>2</sub>膜の上にさらにプラズマCVDにより第3 SiO<sub>2</sub>膜を成膜した状態を示す模式的断面図である。

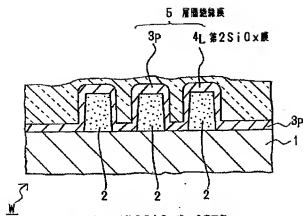
【符号の説明】

1…基板 2…Al系配線パターン 3p…第1 SiO<sub>2</sub>膜 4L…第2 SiO<sub>2</sub>膜 5, 7, 9…層間絶縁膜 6p…改質層 8p…第3 SiO<sub>2</sub>膜 W…ウェハ

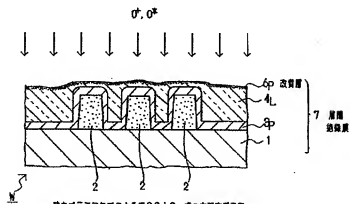
【図1】



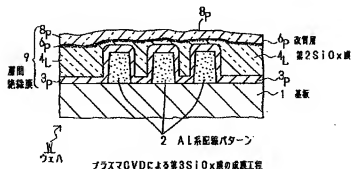
【図2】

LPCVDによる $\text{SiO}_2$ 膜の成膜工程

【図3】

酸素プラズマ処理による $\text{SiO}_2$ 膜の表面改質工程  
(実施例2)

【図4】

プラズマCVDによる $\text{SiO}_2$ 膜の成膜工程